ABSTRACT OF THE DISCLOSURE

Provided is a circuit for use in a semiconductor memory optimized to improve data read ability at low supply voltages. Circuit includes a direct sense AMP circuit, an input/output gate circuit, and an operation control unit. The direct sense AMP circuit transmits read data loaded in a bit line pair including first and second bit lines to a data input/output pair including first and second data input/output lines in response to a read command signal. The input/output gate circuit which, in response to a read/write signal, also passes the read data loaded in the bit line pair directly to the data input/output line pair, and passes write data loaded in the data input/output line pair directly to the bit line pair. The operation control unit which, in response to a column address signal and a write command, generates the read command signal and the read/write signal to turn ON both the direct sense AMP circuit and the input/output gate circuit in a data read operation, or to turn ON the input/output gate circuit and turn OFF the direct sense AMP circuit in a data write operation. Since both a data transmission line and a data write line of a direct sense AMP circuit are activated, resistance to current is reduced and it is possible to perform a data read operation even when a supply voltage is low.